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(54) **Insulated gate bipolar transistor and method of making the same**

(57) An n-type buffer layer (12) and a p-type collector layer (10) are formed on a side of one surface of a semiconductor substrate (11). The p-type collector layer (10) is set to have a low doping dose amount and set shallow so that a low injection efficiency emitter structure for a power semiconductor device is realized. The breakdown voltage of the power device is determined by the thickness of a drift layer (13). A p-type base layer (14), an n-type emitter layer (15) and a p-type base contact layer (16) are formed on a side of the other surface of the semiconductor substrate (11). An n-type low resistance layer (17) reduces a junction FET effect. An emitter electrode (18) comes into contact with the n-type emitter layer (15) and the p-type base contact layer (16). A collector electrode (21) comes into contact with the p-type collector layer (10). A gate electrode (20) is formed on a gate insulating film (19A) above a channel region on a surface portion of the p-type base layer (14).

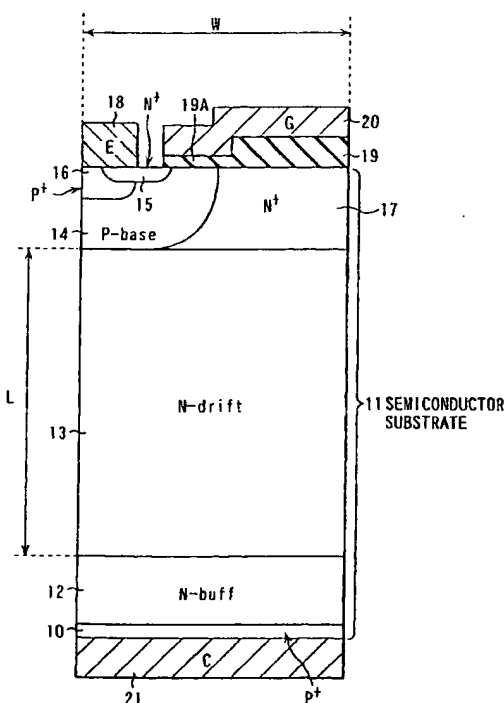


FIG. 2

Description

[0001] The present invention relates to a high voltage semiconductor device, and more particularly, to a power device such as an IGBT.

[0002] A conventional high voltage vertical power device will be explained below while taking the case of a punch through type IGBT using an epitaxial substrate.

[0003] FIG. 1 is a sectional view of a cell area of the conventional punch through type IGBT using the epitaxial substrate.

[0004] The epitaxial substrate comprises a positive semiconductor substrate (positive collector layer) 11 and a negative epitaxial layer formed on the semiconductor substrate 11 by an epitaxial growth method. In this example, the epitaxial layer comprises a negative buffer layer 12 and a N type drift layer (active layer) 13. For example, concentration of positive impurity in the semiconductor substrate 11 is set to about 7.5×10^{18} atoms/cm³, concentration in the negative impurity in the buffer layer 12 is set to about 2.7×10^{17} atoms/cm³, and concentration of negative impurity in the drift layer 13 is set to about 1.35×10^{14} atoms/cm³.

[0005] A positive base layer 14 is formed on a surface region of the drift layer 13. A negative emitter layer 15 and a positive base contact layer 16 are formed in the positive base layer 14. A negative low resistant layer 17 which is adjacent to the positive base layer 14 is formed in the drift layer 13.

[0006] For example, surface concentration of positive impurity in the positive base layer 14 is set to about 4.0×10^{17} atoms/cm³, surface concentration of negative impurity in the negative emitter layer 15 is set to about 1.27×10^{20} atoms/cm³, surface concentration of positive impurity in the positive base contact layer 16 is set to about 2.8×10^{19} atoms/cm³, and surface concentration of negative impurity in the negative low resistant layer 17 is set to about 5.0×10^{15} atoms/cm³.

[0007] An emitter electrode 18 is formed on the negative emitter layer 15 and the positive base contact layer 16. The emitter electrode 18 is in contact with the negative emitter layer 15 and the positive base contact layer 16. A gate electrode 20 is formed on the positive base layer 14 through an insulating film 19. A collector electrode 21 is formed on a back surface of the semiconductor substrate 11.

[0008] In the conventional power device including the above-described IGBT, an epitaxial substrate is employed. However, manufacturing cost of the epitaxial substrate is high and as a result, a cost of the vertical power device is increased.

[0009] In the power device, a so-called life time control is conducted in order to enhance the turn off characteristics. As the life time is shorter, a high speed turn off is possible. Therefore, the life time has been set from a range of 5 to 10 μ s to about 100 ns.

[0010] However, as is well known, the turn off characteristics and the on characteristics are in a relation of

trade-off. That is, if the turn off characteristics is enhanced, ON voltage becomes higher and on characteristics are deteriorated.

[0011] This trade-off relation is generated not only in the above-described punch through type device having the buffer layer, but also in a non-punch through type device having no buffer layer and in a trench gate type device.

[0012] Semiconductor devices according to aspects of first and second inventions comprises: a first conductive type first base layer; a second conductive type collector layer on a side of a first surface of the first base layer; a first conductive type buffer layer between the first base layer and the collector layer; a second conductive type second base layer on a side of a second surface of the first base layer; a first conductive type emitter layer in the second base layer; and a gate electrode 20 above the second base layer between the emitter layer and the first base layer.

[0013] In the semiconductor device of the aspect of the first invention, the first base layer comprises a semiconductor substrate, each of the collector layer, the second base layer and the emitter layer comprises a diffusion layer in the semiconductor substrate, and a depth of diffusion of the collector layer is 1 μ m or less.

[0014] In the semiconductor device of the aspect of the second invention, the following condition is satisfied: $5 \geq \text{BDP} \cdot \text{QP}/\text{bDN} \cdot \text{QN}$ (QN is a dose amount of the buffer layer, bDN is an average of a diffusion coefficient in the buffer layer, QP is a dose amount of the collector layer, and bDP is an average of a diffusion coefficient in the collector layer).

[0015] A manufacturing method of an aspect of a third invention is applied to a semiconductor device in which a power device and its control section are formed in one chip, and comprises a step for implanting impurities into a forming region of the power device and a forming region of the control section at the same time, thereby forming a first impurity layer which becomes a portion of the power device in the forming region of the power device, and a step for forming a second impurity layer which becomes a portion of the control element in the forming region of the control section.

[0016] A manufacturing method of an aspect of a fourth invention is applied to a semiconductor device in which a power device and its control section is formed in one chip, and comprises: a step for forming a conductive film in each of a forming region of a power device and a forming region of a control section, a step for etching the conductive films by RIE using one mask, a step for forming first electrode which becomes a portion of the power device in the forming region of the power device, and a step for forming a second electrode which becomes a portion of the control element in the forming region of the control section.

[0017] This summary of the invention does not necessarily describe all necessary features so that the invention may also be a sub-combination of these de-

scribed features.

[0018] The invention can be more fully understood from the following detailed description when taken in conjunction with the accompanying drawings, in which:

FIG. 1 is a sectional view showing a conventional IGBT;

FIG. 2 is a sectional view showing an IGBT according to a first example of the present invention;

FIG. 3 is a sectional view showing an IGBT according to a second example of the present invention;

FIG. 4 is a view showing a concentration profile of a surface portion of a device shown in FIG. 3;

FIG. 5 is a sectional view showing an IGBT according to a third example of the present invention;

FIG. 6 is a sectional view showing an IGBT according to a fourth example of the present invention;

FIG. 7 is a sectional view showing an IGBT according to a fifth example of the present invention;

FIG. 8 is a sectional view showing a step of a manufacturing method according to a sixth example of the present invention;

FIG. 9 is a sectional view showing a step of a manufacturing method according to the sixth example of the present invention;

FIG. 10 is a sectional view showing a step of a manufacturing method according to the sixth example of the present invention;

FIG. 11 is a sectional view showing a step of a manufacturing method according to the sixth example of the present invention;

FIG. 12 is a sectional view showing a step of a manufacturing method according to the sixth example of the present invention;

FIG. 13 is a sectional view showing a step of a manufacturing method according to the sixth example of the present invention;

FIG. 14 is a sectional view showing a step of a manufacturing method according to the sixth example of the present invention;

FIG. 15 is a sectional view showing a step of a manufacturing method according to the sixth example of the present invention;

FIG. 16 is a sectional view showing a step of a manufacturing method according to the sixth example of the present invention;

FIG. 17 is a sectional view showing a step of a manufacturing method according to the sixth example of the present invention;

FIG. 18 is a sectional view showing a step of a manufacturing method according to the sixth example of the present invention;

FIG. 19 is a sectional view showing a step of a manufacturing method according to the sixth example of the present invention;

FIG. 20 is a sectional view showing a step of a manufacturing method according to the sixth example of the present invention;

FIG. 21 is a sectional view showing an IGBT according to a seventh example of the present invention; FIG. 22 is a view showing a current waveform at the time of turn off;

FIG. 23 is a view showing a current amplification factor (current gain) at the time of turn off;

FIG. 24 is a view showing a relation between electron current and collector current at the time of turn off;

FIG. 25 is a view showing a relation between electron current and collector current at the time of turn off;

FIG. 26 is a view showing a relation between average of impurity density and average of diffusion coefficient; and

FIG. 27 is a view showing one example for obtaining dose amount of negative buffer layer.

[0019] A semiconductor device and its manufacturing method of the present invention will be explained in detail below with reference to the drawings.

1. First Example

[0020] FIG. 2 is a sectional view showing a cell area of a punch through type IGBT according to a first example of the present invention.

[0021] A vertical power device of this example is characterized in that, firstly, a thickness of a positive emitter layer is thin and a low injection efficiency emitter structure (or a low implantation emitter structure or a transference emitter structure) is employed, and secondary, a breakdown voltage of the vertical power device is adjusted by a thickness of N type drift layer (active layer).

[0022] Based on the above characteristics, a concrete structure of the device will be explained.

[0023] A positive collector layer (emitter layer) 10 and a negative buffer layer 12 are formed on one surface (back surface) of a negative semiconductor substrate 11. Each of the positive collector layer 10 and the negative buffer layer 12 is formed by implanting impurities into the semiconductor substrate 11 using ion-implantation.

[0024] A depth (thickness) of the positive collector layer 10 is set to 1.0 μm or less, e.g., in a range of 0.1 to 1.0 μm . A surface concentration of the positive collector layer 10 is set in a range of 2×10^{17} atoms/ cm^3 to 1×10^{20} atoms/ cm^3 . An appropriate surface concentration of the positive collector layer 10 depends on a depth of the positive collector layer 10.

[0025] By forming the positive collector layer 10 by the ion-implantation of low dose amount, and by reducing the depth of the positive collector layer 10, a low injection efficiency emitter structure can be realized.

[0026] The low injection efficiency emitter structure is mainly employed in a non punch through type device having no buffer layer, and has such an operation principle that since implantation amount of holes from the positive

collector layer 10 to a N type drift layer (active layer) 13 to holes is small, high speed turn off can be realized.

[0027] In the present invention, the low injection efficiency emitter structure is employed so as to enhance the turn off characteristics, it is unnecessary to control the life time unlike the prior art and thus, it is possible to prevent the turn off characteristics from being deteriorated by the life time control.

[0028] On the other hand, in order to prevent the vertical power device from being destroyed when reverse bias is applied to the vertical power device, the breakdown voltage of the power device when the device is in the reverse bias state is controlled by the thickness of the N type drift layer (active layer) 13.

[0029] For example, if the impurity density of the N type drift layer (active layer) 13 is set to an appropriate value, it is possible to provide a power device having about 10 μm thickness and having a static breakdown voltage of about 100V. That is, if the thickness of the N type drift layer 13 is set to about 10 μm , the power device has a static breakdown voltage of about 100V, and if the thickness is set to 20 μm , the power device has a static breakdown voltage of about 200V. In generally, if the thickness of the N type drift layer 13 is set to $10 \times I$ (I is an integer) μm , the power device has a static breakdown voltage of about $(100 \times I)\text{V}$.

[0030] In the case of a planer type, if 600V is given to the power device, a relation between the thickness L of the N type drift layer 13 and the half cell size W is set such that $6 \times W$ is equal to or extremely close to L ideally. That is, in order to provide a power device capable of having a static breakdown voltage of about 600V, since $L=60 \mu\text{m}$, the half cell size W is 10 μm .

[0031] In a state in which $L=60 \mu\text{m}$ is secured, if the half cell size W is set to less than 10 μm , improvement (reduction of ON voltage) of element characteristic is rated. This is because that since junction FET resistance between gates is increased, even if the half cell size W is reduced excessively, the on voltage is not reduced. That is, even if a pitch of cell is simply reduced to make the device fine, this does not contribute the reduction of on voltage. On the other hand, in the case of on resistance of the IGBT, since a rate occupied by channel resistance is great, to shorten the channel is effective for reducing the on voltage.

[0032] Taking the above points into account and in order to prevent the device from being destroyed by shortening the channel, and from a result of simulation, the relation between the thickness L of the N type drift layer 13 and the half cell size W is set to such a value that can satisfy $8 \times W > L$. For example, when a power device has a static breakdown voltage of about 600V, the half cell size W can be reduced to 7.5 μm .

[0033] A thickness of the negative buffer layer 12 is set to about 15 μm , and a concentration of negative impurity in the buffer layer 12 is set to about 2.7×10^{17} atoms/ cm^3 . The thickness of the N type drift layer (active layer) 13 is set to about 52.5 μm for example, and a con-

centration of negative impurity in the N type drift layer 13 is set to about 1.35×10^{14} atoms/ cm^3 for example.

[0034] A positive base layer 14 is formed in a surface region of the N type drift layer 13. A negative emitter layer 15 and a positive base contact layer 16 are formed in the positive base layer 14. A negative low resistant layer 17 which is adjacent to the positive base layer 14 is formed in the N type drift layer 13.

[0035] A depth of the positive base layer 14 is set to about 4.5 μm , and a surface concentration of positive impurity in the positive base layer 14 is set to about 4.0×10^{17} atoms/ cm^3 . A depth of the negative emitter layer 15 is set to about 0.3 μm , and a surface concentration of negative impurity in the negative emitter layer 15 is set to about 1.27×10^{20} atoms/ cm^3 .

[0036] A depth of the positive base contact layer 16 is set to about 2.5 μm , and a surface concentration of the positive impurity in the positive base contact layer 16 is set to about 2.8×10^{19} atoms/ cm^3 . A depth of the negative low resistant layer 17 is set to about 4.5 μm , and a surface concentration of negative impurity of the negative low resistant layer 17 is set to about 5.0×10^{15} atoms/ cm^3 .

[0037] An emitter electrode 18 is formed on the negative emitter layer 15 and the positive base contact layer 16. The emitter electrode 18 is in contact with the negative emitter layer 15 and the positive base contact layer 16. A gate electrode 20 is formed on the positive base layer (channel region) 14 through a gate insulating film 19A. A field insulating film 19 having sufficient thickness is formed on the negative low resistant layer 17. A collector electrode 21 is formed on a back surface of the semiconductor substrate 11.

[0038] According to the punch through type IGBT of the first example of the present invention, the positive emitter layer is thin, and a low injection efficiency emitter structure is employed. Therefore, in order to enhance the turn off characteristics, it is unnecessary to control the life time unlike the prior art and thus, it is possible to prevent the turn off characteristics from being deteriorated by the life time control.

[0039] According to the punch through type IGBT of the first example of the present invention, the breakdown voltage is adjusted by the thickness of the N type drift layer (active layer). The on voltage can be reduced by shortening the channel of the IGBT cell, and if the cell is formed such that $8 \times W > L$ is satisfied, the element characteristic can be enhanced (on voltage is reduced) and high voltage operation can be realized at the same time.

2. Second Example

[0040] FIG. 3 is a sectional view of a cell area of a punch through type IGBT of a second example of the present invention.

[0041] A vertical power device of this example is a modification of the punch through type IGBT of the first

example, and includes all the characteristics of the punch through type IGBT of the first example.

[0042] In addition to the characteristics of the punch through type IGBT of the first example, the vertical power device of the second example is characterized in that a positive impurity layer 2 of IGBT cell is added in order to prevent the destruction when the channel of the IGBT cell is shortened.

[0043] For example, when the channel of the IGBT cell is shortened, the channel is prone to be destroyed. Thereupon, in this example, in order to effectively prevent the destruction without changing a threshold value V_{th} of the IGBT cell, a positive impurity layer 22 is formed on the channel portion of the IGBT cell utilizing a CMOS process. A surface concentration of the positive impurity layer 22 is set to such a value that the threshold value V_t of the MOS transistor is not varied. Here, the CMOS process is a manufacturing process of a power device in which ion is implanted into a channel portion using a mask and then, a gate oxide film and a gate electrode are formed. The reason why this process is called CMOS process is that this process applies a process (generally called "CMOS process") used for manufacturing a complementary CMOS transistor, i.e., a generally CMOS process is applied for manufacturing of a power device in this example.

[0044] FIG. 4 shows a concentration profile of impurity of a surface portion (lateral direction) of the IGBT cell area. In the positive base layer 14 which will become a channel of the IGBT cell, a concentration profile of positive impurity in an end of the positive base layer 14 is not constant and is largely inclined. This is because that the positive base layer 14 is formed by ion-implantation and thermal diffusion. As a result, as the channel of the IGBT cell is shortened, the concentration profile of the channel portion is largely inclined as shown in the drawing (solid line). Element destruction such as punch through is prone to be generated.

[0045] Thereupon, in this example, a positive impurity layer 22 is newly formed on the channel portion of the IGBT cell by ion-implantation and thermal diffusion. As a result, the dose amount of the channel portion of the IGBT cell is added, and the concentration profile of the channel portion of the IGBT cell becomes substantially constant (broken line). Therefore, it is possible to prevent the destruction of element, and to reduce the ion voltage by shortening the channel.

[0046] As described above, since the vertical power device of the example has the positive impurity layer 22, the channel resistance can be reduced without changing the threshold value of the IGBT cell, and the on voltage can be reduced. Since a thin semiconductor substrate is used and the low injection efficiency emitter structure is employed in the vertical power device of this example also, it is possible to obtain the effect that the high speed turn off is possible without controlling the life time.

3. Third Example

[0047] FIG. 5 is a sectional view of a cell area of a punch through type IGBT of a third example of the present invention.

[0048] A vertical power device of this example is also a modification of the punch through type IGBT of the first example, and includes all the characteristics of the punch through type IGBT of the first example.

[0049] In addition to the characteristics of the punch through type IGBT of the first example, the vertical power device of the third example is characterized in that the field insulating film 19 on the negative low resistant layer 17 is formed of an LOCOS oxide film.

[0050] For example, in the CMOS process (process used for manufacturing a complementary MOS transistor), the LOCOS oxide film is usually employed for realizing electrical insulation of transistors in the CMOS area. Thereupon, in the vertical power device of this example also, the CMOS process is employed, and electrical isolation of elements using the LOCOS oxide film can be employed.

[0051] A portion of the LOCOS oxide film enters into the semiconductor substrate 11, a sufficient thickness can be secured, it is possible to moderate a step on the semiconductor substrate 11. As a result, a wire can be prevented from being cut oxide film, and resistance can be prevented from increasing.

[0052] In the vertical power device of this example, since the LOCOS oxide film is employed in the field insulating film 19, the step on the semiconductor substrate 11 can be moderated. Since a thin semiconductor substrate is used and the low injection efficiency emitter structure is employed in the vertical power device of this example also, it is possible to obtain the effect that the high speed turn off is possible without controlling the life time.

4. Fourth Example

[0053] FIG. 6 is a sectional view of a cell area of a punch through type IGBT of a fourth example of the invention.

[0054] A vertical power device of this example is a modification of the punch through type IGBT of the third example, and includes all the characteristics of the punch through type IGBT of the third example.

[0055] In addition to the characteristics of the punch through type IGBT of the third example, the vertical power device of the third example is characterized in that a groove 23 is formed in a surface portion of the positive base contact layer 16 to enhance the turn off characteristics. That is, by forming the groove 23 in the surface portion of the positive base contact layer 16, the hole can be discharged smoothly at the time of turn off. Therefore, high speed turn off can be realized.

[0056] The groove 23 can be formed using various methods. For example, when the CMOS process ex-

plained in the third example is employed, the groove 23 can be formed utilizing a step for forming the LOCOS oxide film.

[0057] That is, the LOCOS oxide film 19 is first formed and then, the LOCOS oxide film 19 is etched to form a negative diffusion layer in a peripheral area (region other than a region where IGBT cell is formed). At that time, if an LOCOS oxide film on the positive base contact layer 16 is also etched, the groove 23 is formed.

[0058] The CMOS process will be explained later.

[0059] In this manner, in the vertical power device of this example, the LOCOS oxide film is employed on the field insulating film 19, and the groove 23 is formed in the surface of the positive base contact layer 16 utilizing the step for forming the LOCOS oxide film. With this method, the hole can be discharged smoothly at the time of turn off and therefore, high speed turn off can be realized.

5. Fifth Example

[0060] FIG. 7 is a sectional view of a cell area of a punch through type IGBT of a fifth example of the invention.

[0061] A vertical power device of this example is characterized in that a gate insulating film 19A of the IGBT cell area and a gate insulating film 19B of the peripheral area (control element area) are made of the same material at the same time.

[0062] That is, the vertical power device includes the IGBT cell area and the peripheral area. The peripheral area is formed with a negative channel MOS transistor and a positive channel MOS transistor for controlling action of the cell of the IGBT cell area.

[0063] Therefore, if the CMOS process is employed for manufacturing the vertical power device of this example, the MOS transistor of the peripheral area and the IGBT cell of the IGBT cell area can be formed at the same time.

[0064] This example can be applied not only to the punch through type device having the buffer layer, but also to a non-punch through type device or a trench gate type device. This example can be applied to both the vertical power device and a horizontal power device.

[0065] A concrete example of a manufacturing method of the power device of this example will be explained below.

[0066] First, as shown in FIG. 8, an oxide film 31 is formed on the negative semiconductor substrate (which will become a N type drift layer 13) 11 by thermal oxidation.

[0067] As shown in FIG. 9, a resist pattern is formed on an oxide film 31 by PEP (Photo Engraving Process), this resist pattern is used as a mask and the oxide film 31 of the IGBT cell area is removed by RIE. After the resist pattern was removed, negative impurities (e.g., phosphorus) are implanted into the semiconductor substrate 11 by ion-implantation.

[0068] Next, as shown in FIG. 10, an oxide film 32 is formed on the semiconductor substrate 11 again by thermal oxidation. At that time, the negative low resistant layer 17 is formed in the semiconductor substrate 11.

[0069] Next, as shown in FIG. 11, a resist pattern is formed on the oxide film 31, and the oxide film 31 of the peripheral area is partially removed using this resist pattern as a mask. Then, the resist pattern is removed, a thin oxide film 33 which suppresses damage at the time of ion-implantation is formed on the exposed semiconductor substrate 11 on the peripheral area. Then, positive impurities (such as boron) are implanted into the semiconductor substrate 11 by ion-implantation.

[0070] Next, as shown in FIG. 12, a positive impurity layer 35 is formed in the semiconductor substrate 11 by thermal oxidation and diffusion.

[0071] Then, as shown in FIG. 13, a resist pattern is formed on the oxide film 34 by PEP, and the oxide film 34 in the IGBT cell area and the peripheral area is removed using the resist pattern as a mask.

[0072] Then, as shown in FIG. 14, the resist pattern is removed, thin oxide film which suppresses damage at the time of ion-implantation is formed on the exposed semiconductor substrate 11 on the IGBT cell area and the peripheral area. Then, positive impurities (such as boron) are implanted into the semiconductor substrate 11 by ion-implantation.

[0073] Then, as shown in FIG. 15, the positive impurity layer (positive base layer) 14 is formed in the semiconductor substrate 11 by the thermal oxidation and diffusion.

[0074] Next, the oxide film of the IGBT cell area is removed, and thin oxide film which suppresses damage at the time of ion-implantation is formed. Then, positive impurities (such as boron) are implanted into the semiconductor substrate 11 by ion-implantation.

[0075] Next, as shown in FIG. 16, a positive impurity layer (so-called negative channel implantation layer) 36 is formed in the semiconductor substrate 11 by thermal oxidation and diffusion.

[0076] Then, as shown in FIG. 17, a thin oxide film (gate oxide film) is formed on the semiconductor substrate 11 by thermal oxidation.

[0077] Thereafter, a polysilicon film is formed on the entire surface. A resist pattern is formed on the polysilicon film by PEP, and the resist pattern is used as a mask to etch the polysilicon film. As a result, the IGBT cell area is formed with a gate electrode 20.

[0078] Next, as shown in FIG. 18, using the resist pattern as a mask, positive impurities (e.g., boron) are implanted into the semiconductor substrate 11 by ion-implantation. The, another resist pattern is used as a mask, negative impurities (e.g., arsenic) are implanted into the semiconductor substrate 11 by ion-implantation. At that time, oxide film is peeled off and an oxide film having appropriate thickness is formed before the ion-implantation.

[0079] Then, as shown in FIG. 19, the resist pattern

is removed and then, thermal diffusion is carried out. As a result, the positive base contact layer 16 and the negative emitter layer 15 are formed in the semiconductor substrate 11.

[0080] Next, as shown in FIG. 20, an oxide film 38 is formed on the entire surface. A resist pattern is formed on the oxide film 38 by PEP, and the oxide film 38 is etched using the resist pattern as a mask, thereby forming a contact hole. An electrode (e.g., aluminum) is formed on the oxide film 38 and patterning is carried out, the emitter electrode 18 and other electrode 39 are formed.

[0081] By carrying out the above steps, a structure of one surface of the vertical power device of the present invention is completed.

[0082] A structure of the other surface (back surface) of the vertical power device of the invention can be realized by a step for activating the ion implanted in the semiconductor substrate 11 such as ion-implantation, thermal diffusion or laser annealing. The structure of the back surface can also be realized utilizing the epitaxial substrate.

[0083] According to such a manufacturing method, the IGBT cell area and its control circuit (e.g., circuit made of polysilicon) can be formed by the same process (common process) by employing the CMOS process. Therefore, the number of manufacturing steps is not largely increased, and the manufacturing cost can be reduced.

[0084] The manufacturing method (CMOS process) according to the present invention can be applied not only the vertical power device, but also to the horizontal power device (e.g., manufacturing method of high voltage IPD (Intelligent Power Device) by SOI-CMOS process in which element separation of LOCOS oxide film).

6. Sixth Example

[0085] FIG. 21 is a sectional view of a cell area of a punch through type IGBT of a sixth example of the invention.

[0086] The positive collector layer (emitter layer) 10 and the negative buffer layer 12 are formed on one surface (back surface) of the negative semiconductor substrate 11. The positive collector layer 10 and the negative buffer layer 12 are formed by implanting impurities into the semiconductor substrate 11 using ion-implantation.

[0087] In the device of this example, a low injection efficiency emitter structure is employed like the device of the first example. That is, a surface concentration of the positive collector layer 10 is set in a range of 1×10^{18} atoms/cm³ to 1×10^{20} atoms/cm³, and a depth (thickness) of the positive collector layer 10 is set to 0.1 to 1.0 μm .

[0088] A thickness of the N type drift layer (active layer) 13 is set to a predetermined value in accordance with voltage (specification). For example, when a power de-

vice capable of withstanding 600V, the thickness of the N type drift layer (active layer) 13 is set to about 60 μm .

[0089] The positive base layer 14 is formed in a surface region of the N type drift layer 13. The negative emitter layer 15 and the positive base contact layer 16 are formed in the positive base layer 14. The negative low resistant layer 17 which is adjacent to the positive base layer 14 is formed in the N type drift layer 13. The negative low resistant layer 17 is provided for reducing J (junction) FET effect.

[0090] The emitter electrode 18 is formed on the negative emitter layer 15 and the positive base contact layer 16. The emitter electrode 18 is in contact with the negative emitter layer 15 and the positive base contact layer 16. The gate electrode 20 is formed on the positive base layer (channel region) 14 through the gate insulating film 19A. The gate electrode 20 is covered with the insulating film 19B. With this short circuit between the emitter electrode 18 and the gate electrode 20 is prevented. The collector electrode 21 is formed on a back surface of the semiconductor substrate 11.

[0091] In the above-described IGBT, a negative channel MOS transistor comprises the N type drift layer 13, the positive base layer 14, the negative emitter layer 15, the gate insulating film 19A and the gate electrode 20. If on voltage is applied to the gate electrode 20, a channel is formed in a surface of the positive base layer 14, and electron is implanted into the N type drift layer 13 from the negative emitter layer 15.

[0092] Next, operation of the IGBT will be explained.

[0093] The turn on operation is as follows.

[0094] First, in a state in which collector voltage VCE is applied between the emitter electrode 18 and the collector electrode 21, if a predetermined positive gate voltage (on voltage) VGE is applied between the emitter electrode 18 and the gate electrode 20, the conductive type of the surface region (channel region) of the positive base layer 14 is reversed from positive to negative, and a negative channel is formed. Electron is implanted from the negative emitter layer 15 to the N type drift layer (base layer) 13 through this channel.

[0095] The electron implanted into the N type drift layer 13 is biased through a diode comprising the positive collector layer 10 and the N type drift layer 13 sandwiching the negative buffer layer 12 in the normal direction and thus, the hole is implanted into the N type drift layer 13 from the positive collector layer 10 through the negative buffer layer 12.

[0096] As a result, resistance of the N type drift layer 13 is largely reduced by the modulation of conductivity, and main current flows between the emitter electrode 18 and the collector electrode 21.

[0097] The turn off operation is as follows.

[0098] First, potential lower than that of the emitter electrode 18, e.g., negative potential when the potential of the emitter electrode 18 is 0V, is applied to the gate electrode 20. With this, the negative channel (reversed layer) formed on the surface region (channel region) of

the positive base layer 14 is eliminated, and the implantation of electron from the negative emitter layer 15 to the N type drift layer (base layer) 13 is stopped.

[0099] As a result, a portion of holes accumulated in the N type drift layer 13 is discharged into the emitter electrode 18 through the positive base layers-14 and 16, and a portion of remaining holes is coupled to the electron again. Therefore, the main current flowing between the emitter electrode 18 and the collector electrode 21 is cut off.

[0100] As shown in equation (1), the current amplification factor hFE is defined as being a value obtained by subtracting electron current I_e from collector current I_c .

$$hFE = I_c / I_e \quad (1)$$

[0101] In this case, the present inventor found that a maximum value of the current amplification factor hFE is varied by a dose amount of the negative buffer layer 12 and its thickness and by a dose amount of the positive collector layer 10 and its thickness, and that the maximum value of the current amplification factor hFE is closely related to fall time t_f .

[0102] This point will be explained in detail below.

[0103] FIG. 22 shows a current waveform at the time of turn off, a vertical axis shows current value, and a lateral axis shows time.

[0104] A current waveform ① is of a device in which a thickness of a negative buffer layer is set to 1.2 μm , its dose amount is set to 1.8×10^{13} atoms/ cm^3 , a thickness of a positive collector layer is set to 0.3 μm , and its dose amount is set to 6.2×10^{13} atoms/ cm^3 .

[0105] A current waveform ② is of a device in which the thickness of the negative buffer layer is set to 1.2 μm , its dose amount is set to 1.8×10^{13} atoms/ cm^3 , the thickness of the positive collector layer is set to 0.3 μm and its dose amount is set to 2.2×10^{14} atoms/ cm^3 .

[0106] That is, the ① and ② show current waveforms of two kinds of device in which the thickness and the dose amount of the negative buffer layer and the thickness of the positive collector layer are fixed, and the dose amount of the positive collector layer is varied.

[0107] From FIG. 2, if a fall time t_f of each device is obtained, $t_f=143$ nsec in the case of ① (when the dose amount of the positive collector layer is 2.2×10^{14} atoms/ cm^3), and $t_f=395$ nsec in the case of ② (when the dose amount of positive collector layer is 6.2×10^{13} atoms/ cm^3).

[0108] As described above, it is found that the fall time t_f is varied depending upon variation of the dose amount of the positive collector layer. A cause of variation in the fall time t_f depending upon the variation of the dose amount of the positive collector layer will be explained below.

[0109] FIG. 23 shows transition with time of the current amplification factor hFE at the time of turn off, a ver-

tical axis shows the current amplification factor hFE and a horizontal axis shows time.

[0110] Here, ① is a waveform when a condition is the same as that of the current waveform of ① in FIG. 22, ② is a waveform when a condition is the same as that of the current waveform of ② in FIG. 22. That is, the waveform of ① shows a case in which the dose amount of the positive collector layer is 6.2×10^{13} atoms/ cm^3 , and the current waveform of ② shows a case in which the dose amount of the positive collector layer is 2.2×10^{14} atoms/ cm^3 . The horizontal axis (time) in FIG. 23 corresponds to that shown in FIG. 22.

[0111] From FIG. 22, it is found that when the current value is substantially constant (near 15A in FIG. 22), the current amplification factors hFE of ① and ② are substantially constant, and there is almost no difference between the current amplification factor hFE of ① and the current amplification factor hFE of ②.

[0112] However, if the reduction of current value is started by the turn off operation, the current amplification factor hFE is gradually increased. If the variation the current amplification factor hFE is compared between the ① and ②, it is found that the current amplification factor hFE of ② having long fall time t_f (or turn off period) is greater than the current amplification factor hFE of ① having short fall time t_f (or turn off period).

[0113] That is, the maximum value of the current amplification factor hFE of ① is about three, the maximum value of the current amplification factor hFE of ② is about eight.

[0114] Further, electron current during turn off process when the current amplification factor hFE becomes the maximum value is small as compared with electron current at the normal time, but if the maximum value of the current amplification factor hFE becomes about eight like the case of ②, the collector current I_c becomes eight times greater than the electron current I_e , which is a cause of elongating the turn off period.

[0115] The relation between the maximum value of the current amplification factor hFE and the fall time t_f (or turn off period) will be explained in more detail.

[0116] FIGS. 24 and 25 show current waveforms of the electron current I_e and the collector current I_c at the time of turn off. In each the drawing, the vertical axis shows a current value and horizontal axis shows time.

[0117] FIG. 24 shows waveform corresponding to the condition of ① shown in FIGS. 22 and 23, and FIG. 25 shows waveform corresponding to condition of ② shown in FIGS. 22 and 23. The horizontal axes of FIGS. 24 and 25 correspond to horizontal axes (time) in FIGS. 22 and 23.

[0118] A variation range of the current amplification factor hFE of ① is about 1.6 to 3 (maximum value 3 is generated in a tail portion of current waveform, i.e., near 420 nsec) as shown in FIG. 23. An amplification ratio of the collector current I_c to the electron current I_e is relatively small as shown in FIG. 24, and as a result, the fall time t_f (or turn off period) can be shortened as shown in

FIG. 22.

[0119] Whereas, a variation range of the current amplification factor hFE of ② is about 1.8 to 8 (maximum value 8 is generated in a tail portion of current waveform, i.e., near 800 nsec) as shown in FIG. 23. An amplification ratio of the collector current Ic to the electron current Ie is relatively great as shown in FIG. 25, and as a result, the fall time tf (or turn off period) can be largely elongated.

[0120] As explained above, it is found that during the turn off process, the maximum value of the current amplification factor hFE is varied depending upon the dose amount of the positive collector layer, and this current amplification factor hFE is closely related to the fall time tf (or turn off period).

[0121] Here, in the power device including IGBT shown in FIG. 21, it is required to shorten the fall time tf to a constant value or less. In generally, it is required that the fall time tf is near 200 nsec or less. This is because that by setting the fall time tf to that value, turn off loss (turn off power dissipation) Eoff can be reduced (1 mJ or lower value).

[0122] The present inventor studied the best value of the current amplification factor hFE at the time of turn off using simulation results. As a result, the inventor found that if the current amplification factor hFE at the time of turn off is set to 5 or less, the above-described requirement is satisfied.

[0123] That is, if the power device is manufactured such as to satisfy the condition that the current amplification factor hFE at the time of turn off is 5 or less, the fall time tf can be set to a sufficient short value (e.g., near 200 nsec or shorter), and the turn off loss Eoff can be sufficiently reduced (e.g., 1 mJ or lower).

[0124] Next, a way for manufacturing a power device which satisfies the condition that the current amplification factor hFE at the time of turn off is 5 or less will be explained.

[0125] In the above-described simulation, in the punch through type IGBT, the dose amount and thickness of the negative buffer layer and the thickness of the positive collector layer were fixed, and the dose amount of the positive collector layer was varied.

[0126] However, as a result of more detailed study, it was found that the current amplification factor hFE at the time of turn off is varied depending upon the dose amount and the thickness of the negative buffer layer as well as the dose amount and the thickness of the positive collector layer.

[0127] Grounds of this will be explained below.

[0128] The current amplification factor hFE can be expressed in the following equation (2) under the conditions that the life time is sufficiently long (1 μs to 10 μs), the dose amount of the negative buffer layer is defined as QN, the average of the diffusion coefficient in the negative buffer layer is defined as bDN, the dose amount of the positive collector layer is defined as QP, and the average of diffusion coefficient in the positive collector layer

is defined as bDP.

$$hFE = bDP \cdot QP / bDN \cdot QN \quad (2)$$

[0129] Here, there is a constant relation as shown in FIG. 26 between the average bNbuffer of the impurity density in the negative buffer layer and the average bDN of the diffusion coefficient, and between the average bNcollector of impurity density in the positive collector layer and the average bDP of the diffusion coefficient.

[0130] Further, the average bNbuffer of the impurity density in the negative buffer layer and the average bNcollector of the impurity density in the positive collector layer can be expressed by the equations (3a) and (3b).

$$bNbuffer = \frac{QN}{WN} \quad (3a)$$

$$QN = \int_0^{WN} Nbuffer(x) dx$$

$$bNcollector = \frac{QP}{WP} \quad (3b)$$

$$QP = \int_0^{WP} Ncollector(x) dx$$

[0131] Here, WN represents a thickness of the negative buffer layer, WP represents a thickness of the positive collector layer, Nbuffer(x) represents concentration profile of the negative buffer layer in its depth direction (direction x), and Ncollector(X) represents a concentration profile of the positive collector layer in its depth direction (direction x).

[0132] That is, according to the relations shown in the equations (2), (3a) and (3b), the current amplification factor hFE at the time of turn off can be controlled by the dose amount QN (or concentration profile Nbuffer(x)) and thickness WN of the negative buffer layer, and the dose amount QP (or concentration profile Ncollector(x)) and the thickness WP of the positive collector layer.

[0133] It was confirmed that the two cases ① and ② in the above simulation result also satisfied the equations (2), (3a) and (3b).

[0134] Therefore, the dose amount and the thickness of the negative buffer layer and the dose amount and the thickness of the positive collector layer are determined such as to satisfy the condition that the current amplification factor hFE at the time of turn off is five or less, and a power device is manufactured, the fall time tf can be sufficiently shortened, and the turn off loss Eoff can be made small sufficiently.

[0135] When at least one of the dose amount and the

thickness of the negative buffer layer and the dose amount and the thickness of the positive collector layer is determined, other values which are not yet determined can be determined such as to satisfy the condition that the current amplification factor hFE at the time of turn off is five or less.

[0136] For example, when the dose amount QN of the negative buffer layer is determined (e.g., a peak value of the concentration profile $N_{buffer}(x)$ is set to 5×10^{16} atoms/cm³ or higher), the thickness WN of the negative buffer layer or the dose amount QP and thickness WP of the positive collector layer can be determined.

[0137] When the thickness of the semiconductor substrate (wafer) is determined (e.g., about 70 μm or less), this value is taken into account and the thickness of the negative buffer layer and the thickness of the positive collector layer can be determined.

[0138] When the dose amount QN of the negative buffer layer is determined, determination is made in accordance with the following definition. That is, as shown in FIG. 27, the area of the negative buffer layer 12 is first defined from a boundary between the positive collector layer 10 and the negative buffer layer 12 to a boundary between the negative buffer layer 12 and the N type drift layer 13. The boundary between the negative buffer layer 12 and the N type drift layer 13 is set to a point where the concentration of negative impurity is substantially constant. Then, the dose amount QN of the negative buffer layer is defined as meaning the dose amount of the negative impurity in the negative buffer layer 12 which was defined above.

[0139] In the first to sixth examples, the conductive type of each of the layers constituting the power device is only one example, and the effect of the present invention can of course be obtained even in a device having the reversed conductive type of each layer for example.

[0140] As explained above, according to the present invention, firstly, the thin positive collector layer of low dose amount is formed by ion-implantation, and pressure resistance is secured by the N type drift layer. Therefore, low manufacturing cost can be realized, and the off characteristic can be enhanced without deteriorating the on characteristic.

[0141] Secondary, since the CMOS process is employed to manufacture the power device, the cell area and the control section can be formed using the same process, the number of manufacturing steps (or the number of PEPs) and thus, the low manufacturing cost can be realized.

[0142] Thirdly, the dose amount and the thickness of the negative buffer layer and the dose amount and the thickness of the positive collector layer are determined such that the current amplification factor at the time of turn off becomes five or less. Therefore, the fall time can be shortened sufficiently, and the turn off loss can be made small sufficiently.

Claims

1. A semiconductor device comprising:

a first conductive type first base layer (13);
a second conductive type collector layer (10) on a side of a first surface of said first base layer (13);
a first conductive type buffer layer (12) between said first base layer and said collector layer;
a second conductive type second base layer (14) on a side of a second surface of said first base layer (13);
a first conductive type emitter layer (15) in said second base layer (14); and
a gate electrode 20 above said second base layer (14) between said emitter layer (15) and said first base layer (13);

characterized in that said first base layer (13) comprises a semiconductor substrate, a thickness of said collector layer (10) is set to 1 μm or less.

2. The semiconductor device according to claim 1:

characterized in that each of said collector layer (10), said second base layer (14) and said emitter layer (15) comprises a diffusion layer in said semiconductor substrate, a thickness of said collector layer (10) is defined by a depth of said collector layer (10) from said first surface of said first base layer (13).

3. The semiconductor device according to claim 1:

characterized by further comprising a second conductive type impurity layer disposed in said second base layer (14) between said emitter layer (15) and said first base layer (13), said second conductive type impurity layer (22) is different from said second base layer (14).

4. The semiconductor device according to claim 3:

characterized in that said second base layer (14) between said emitter layer (15) and said first base layer (13) becomes a channel region of a field-effect transistor.

5. The semiconductor device according to claim 1:

characterized in that said second base has a groove, and said emitter layer (15) is disposed along an edge of said groove.

6. The semiconductor device according to claim 1:

characterized by further comprising a first conductive type low resistant layer (17) in said first base layer (13) adjacent to said second base layer (14) and having a resistant value lower than that of said first base layer (13).

7. The semiconductor device according to claim 1:
characterized in that in a condition that a thickness of said first base layer (13) is defined as L, a cell comprises said first base layer (13), said collector layer (10), said buffer layer (12), said second base layer (14), said emitter layer (15) and said gate electrode (20), and a half size of said cell is defined W, the following relation is satisfied:

$$8 \times W > L$$

8. The semiconductor device according to claim 7:
characterized in that a thickness of said semiconductor substrate is 70 μm or less.
9. The semiconductor device according to claim 1:
characterized in that said semiconductor device is an IGBT.

10. A semiconductor device comprising:

a first conductive type first base layer (13);
 a second conductive type collector layer (10) on a side of a first surface of said first base layer (13);
 a first conductive type buffer layer (12) between said first base layer (13) and said collector layer (10);
 a second conductive type second base layer (14) on a side of a second surface of said first base layer (13);
 a first conductive type emitter layer (15) in said second base layer (14); and
 a gate electrode (20) above said second base layer (14) between said emitter layer (15) and said first base layer (13);

characterized in that the following condition is satisfied:

$$5 \geq \text{bDP} \cdot \text{QP} / \text{bDN} \cdot \text{QN}$$

(QN is a dose amount of said buffer layer (12), bDN is an average of a diffusion coefficient in said buffer layer (12), QP is a dose amount of said collector layer (10), and bDP is an average of a diffusion coefficient in said collector layer (10)).

11. The semiconductor device according to claim 10:
characterized in that said first base layer (13) comprises a semiconductor substrate, each of said collector layer (10), said second base layer (14) and said emitter layer (15) comprises a diffusion layer in said semiconductor substrate, a thickness of said collector layer (10) is set to 1 μm or less.

12. The semiconductor device according to claim 10:
characterized in that a thickness of said semiconductor substrate is 70 μm or less.

13. The semiconductor device according to claim 10:
characterized in that a peak value of an impurity density in said buffer layer (12) is set to 5×10^{16} atoms/ cm^3 or higher.

14. The semiconductor device according to claim 10:
characterized in that said semiconductor device is an IGBT.

15. A manufacturing method of a semiconductor device comprising steps of:

forming a power device including a first impurity layer (15, 16); and
 forming a control element including a second impurity layer (18B);

characterized by comprising steps of:

implanting impurities into a power device area and a control element area by ion-implantation using one mask, and forming said first impurity layer (15, 16) in said power device area and said second impurity layer (18B) in said control element area;

16. The manufacturing method according to claim 15:
characterized in that said impurity is negative impurity, said first impurity layer is an emitter layer of an IGBT, and said second impurity layer is a source/drain region of a negative channel field-effect transistor.

17. The manufacturing method according to claim 15:
characterized in that said impurity is positive impurity, said first impurity layer is a collector layer of an IGBT, said second impurity layer is a source/drain region of a positive channel field-effect transistor.

18. The manufacturing method according to claim 15:
characterized in that said impurity is negative impurity, said first impurity layer (15, 16) is an emitter layer (15) of the IGBT, said second impurity layer (18B) is a collector region and an emitter region of an NPN type bipolar transistor.

19. The manufacturing method according to claim 15:
characterized in that said impurity is positive impurity, said first impurity layer is a collector layer of an IGBT, and said second impurity layer is an emitter region and a collector region of a PNP type bipolar transistor.

20. The manufacturing method according to claim 16, 17, 18 or 19:

characterized in that said IGBT is of horizontal type.

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21. A manufacturing method of a semiconductor device comprising steps of:

forming a conductive film on each of a power device area and a control element area, etching
said conductive film by RIE, forming a first electrode (18, 20) in said power device area, forming a second electrode (20B) in said control element area;
forming a power device including said first electrode (18, 20); and
forming a control element including said second electrode (20B).

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22. The manufacturing method according to claim 21:

characterized in that said first electrode is a gate electrode of an IGBT, said second electrode is a gate electrode of a field-effect transistor.

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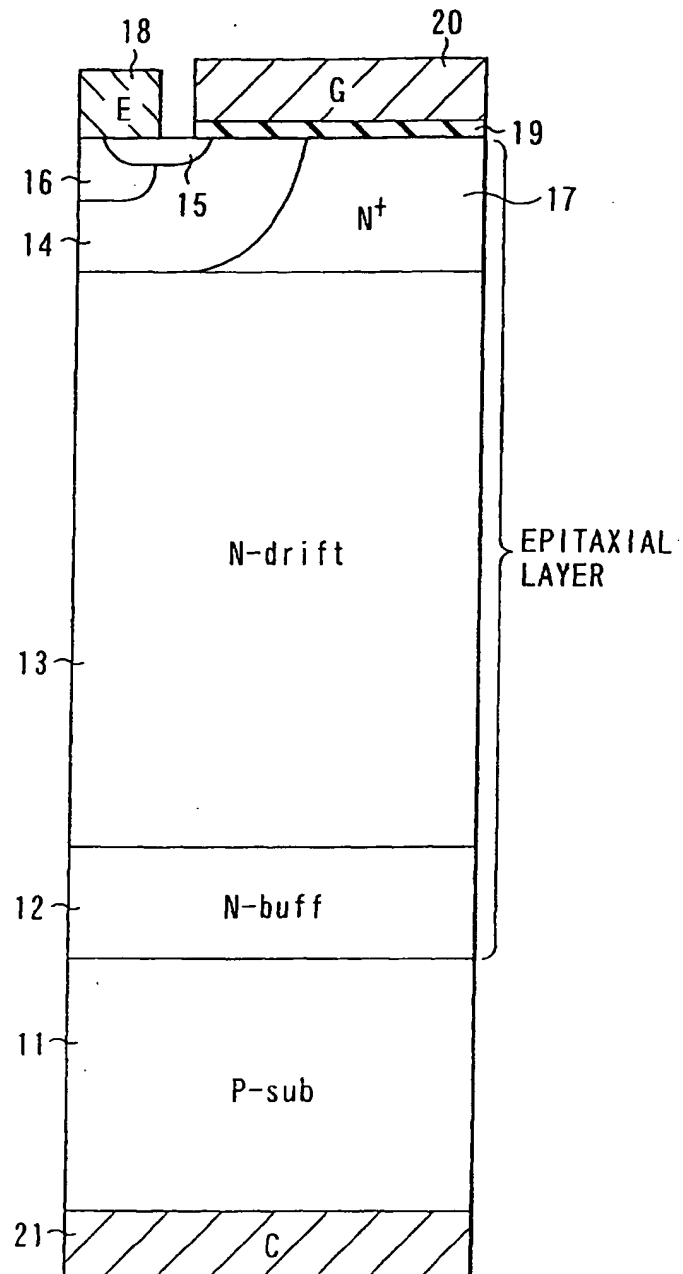


FIG. 1

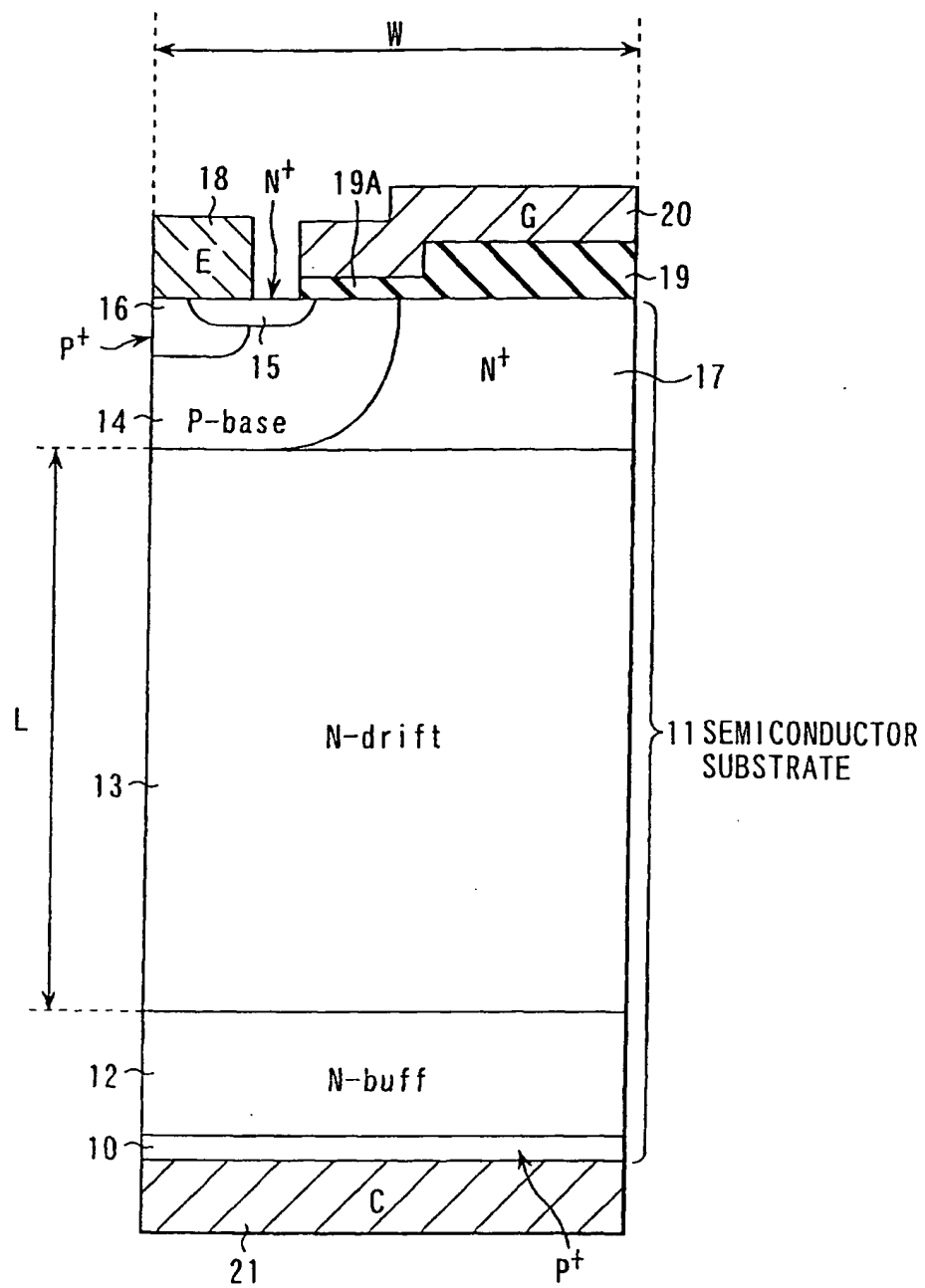


FIG. 2

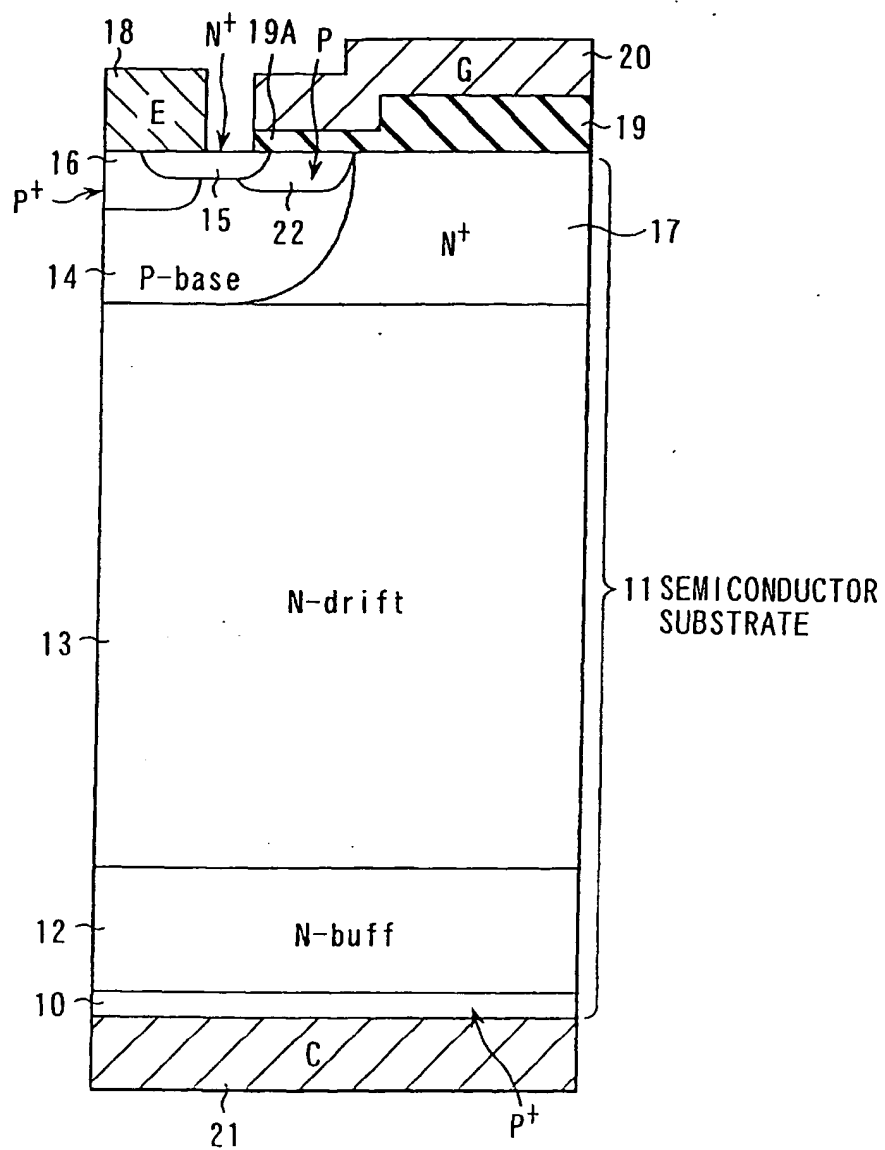


FIG. 3

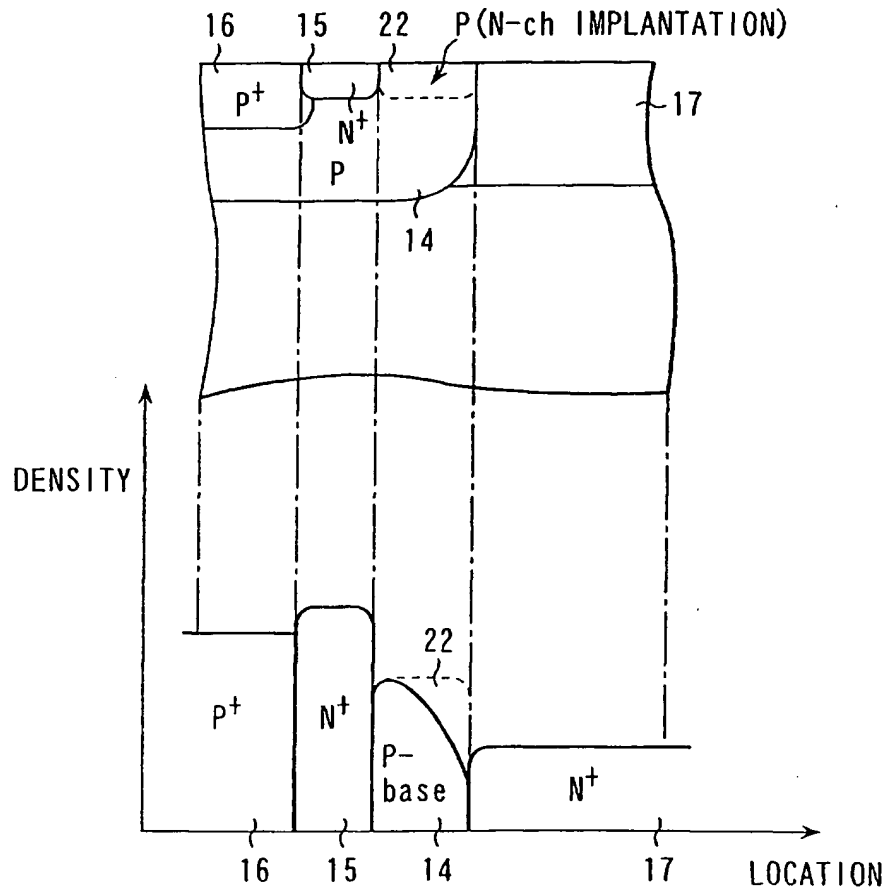


FIG. 4

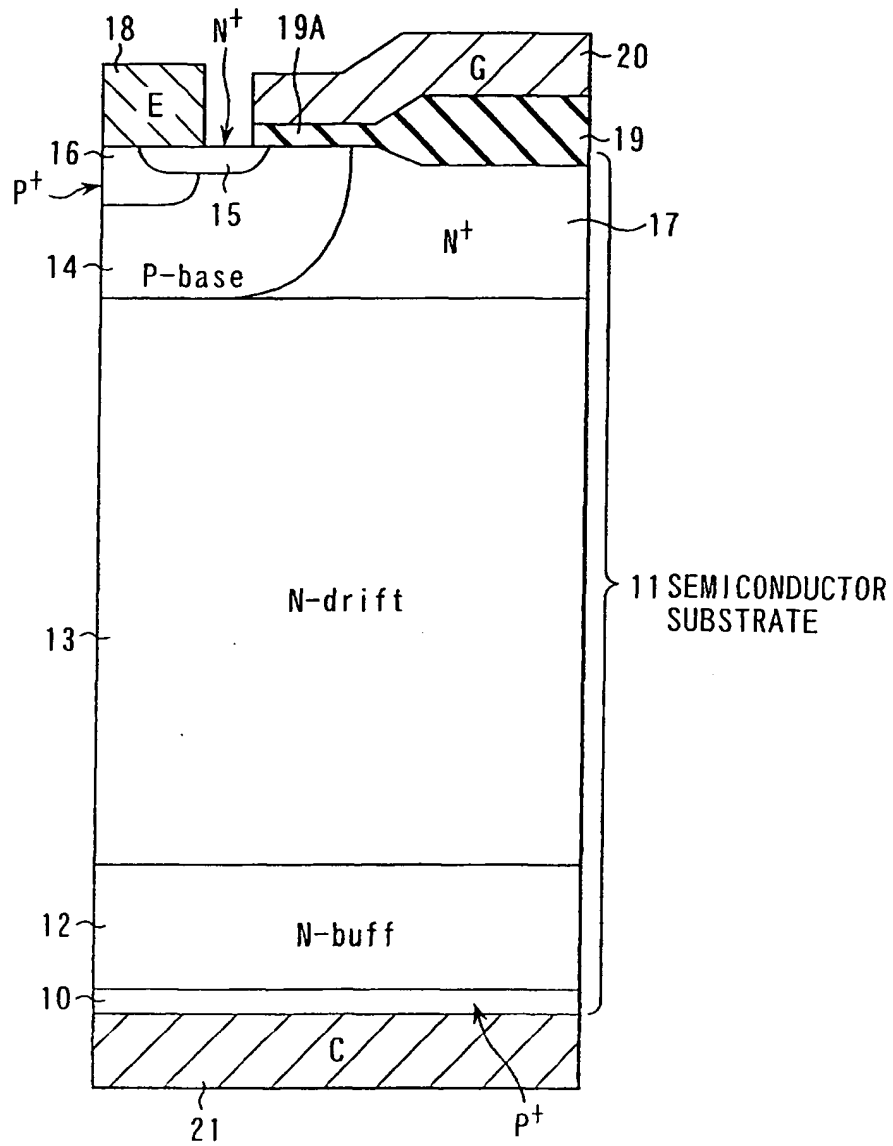


FIG. 5

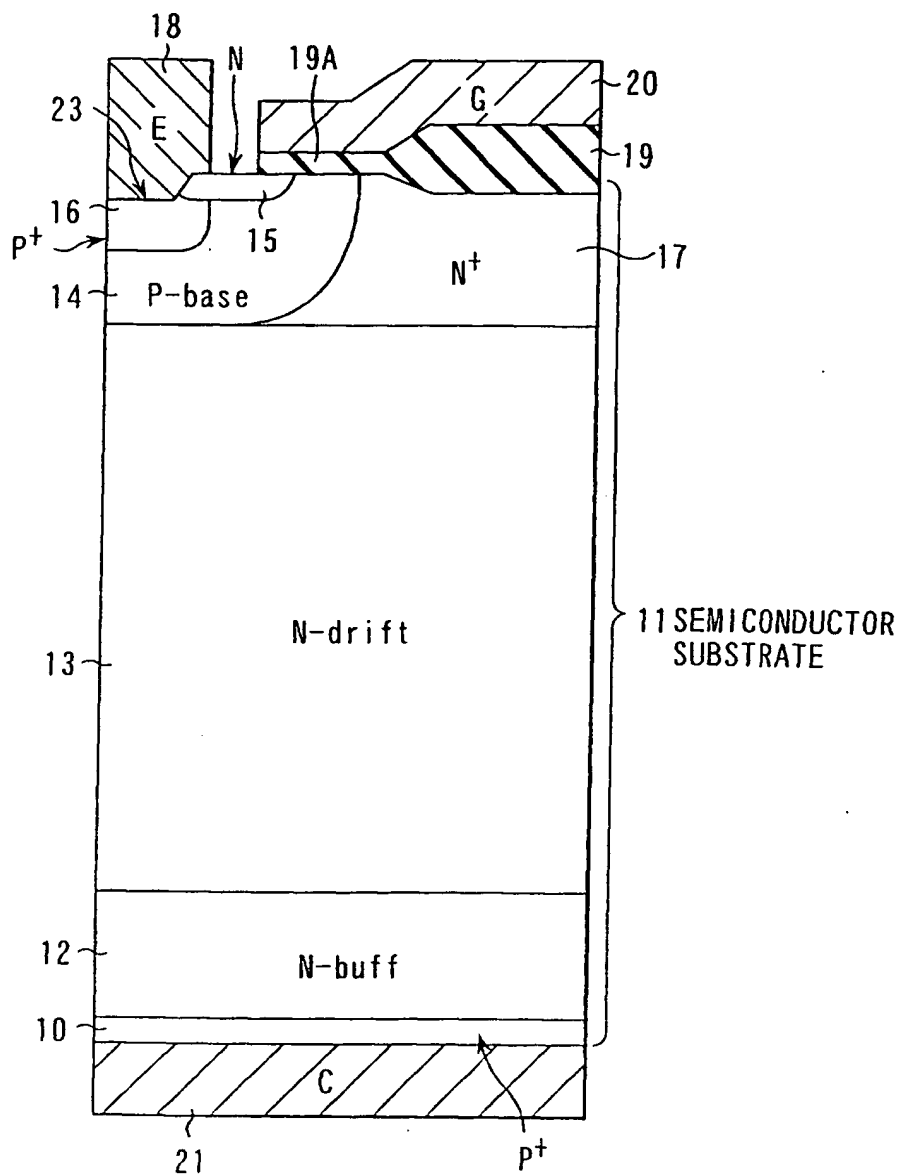
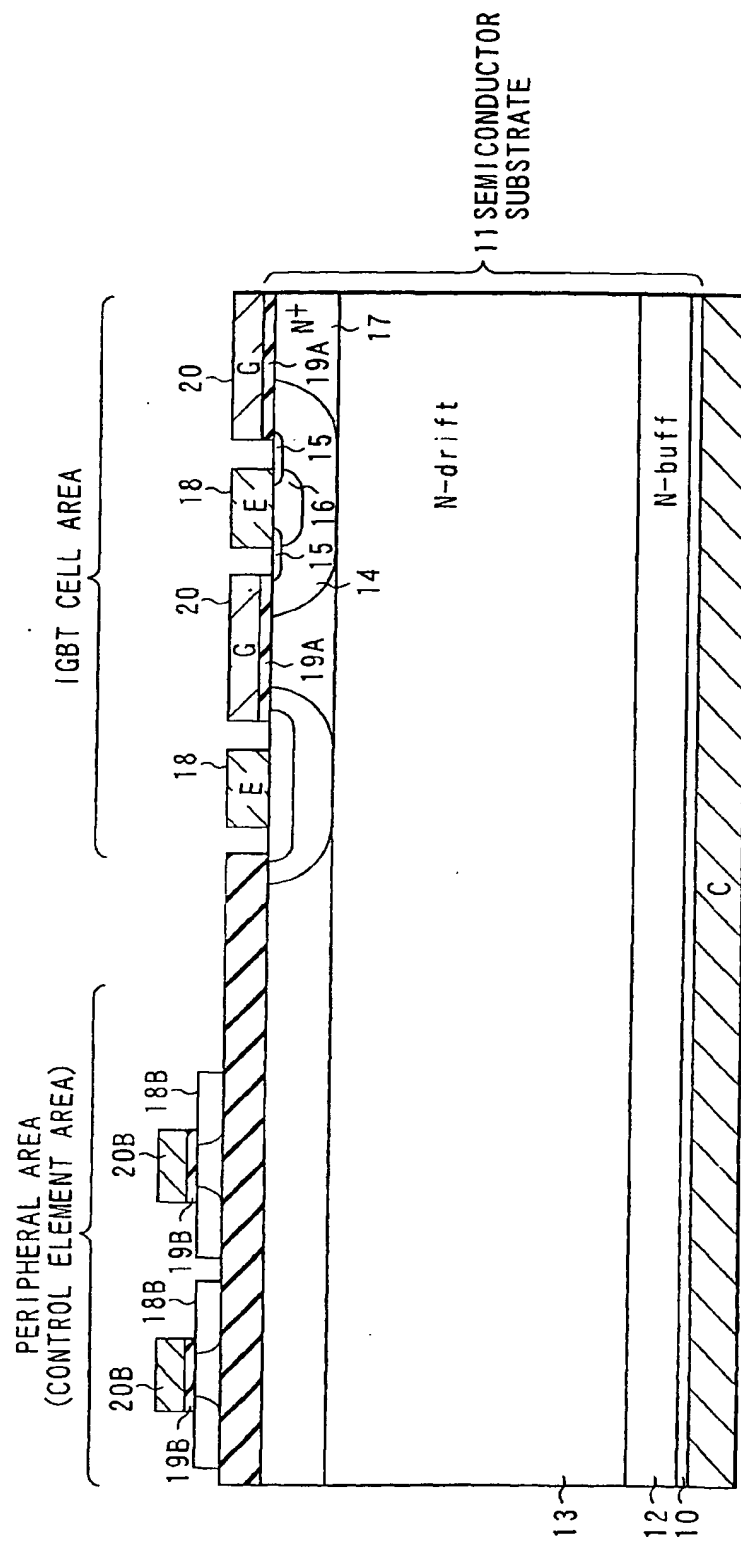


FIG. 6



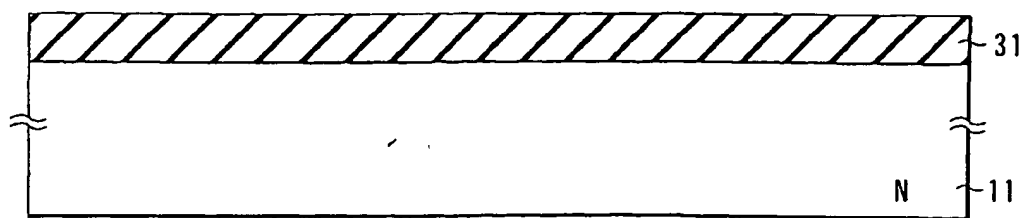


FIG. 8

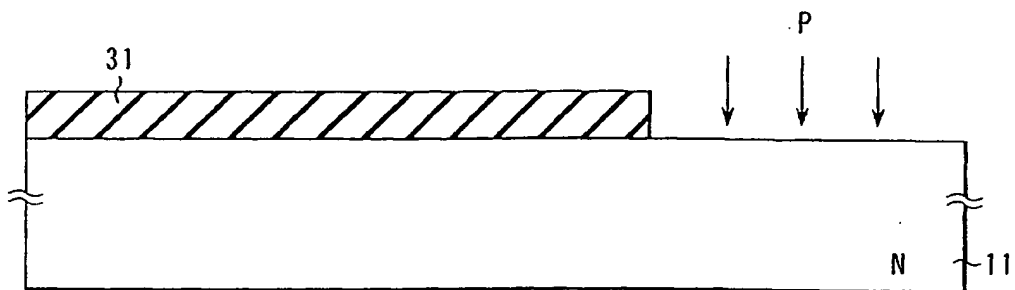


FIG. 9

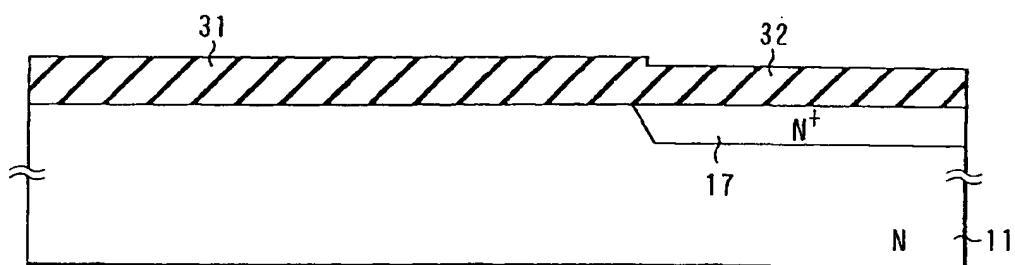


FIG. 10

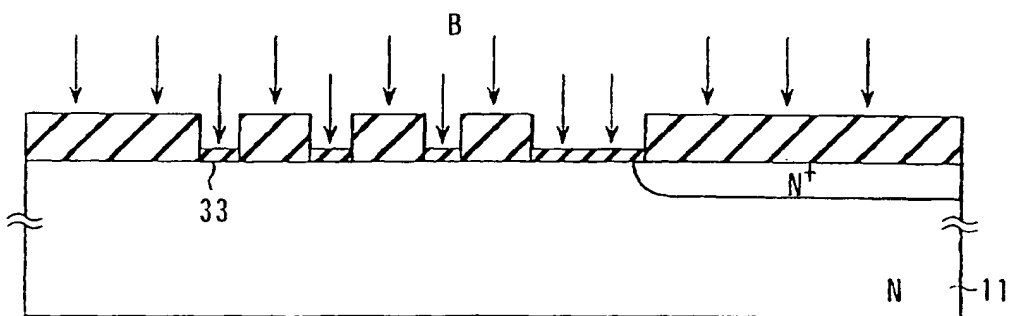


FIG. 11

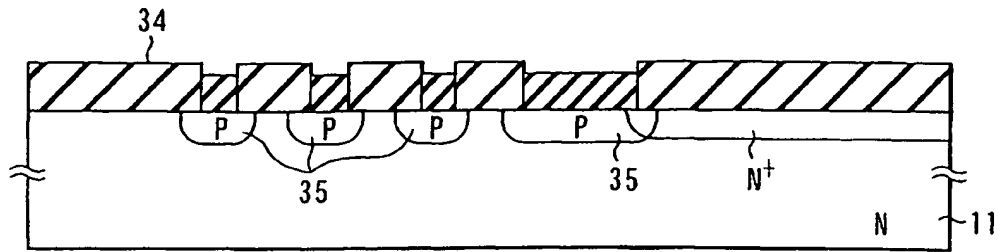


FIG. 12

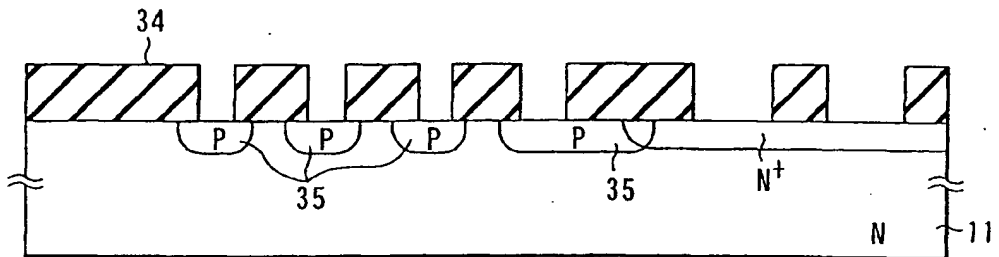


FIG. 13

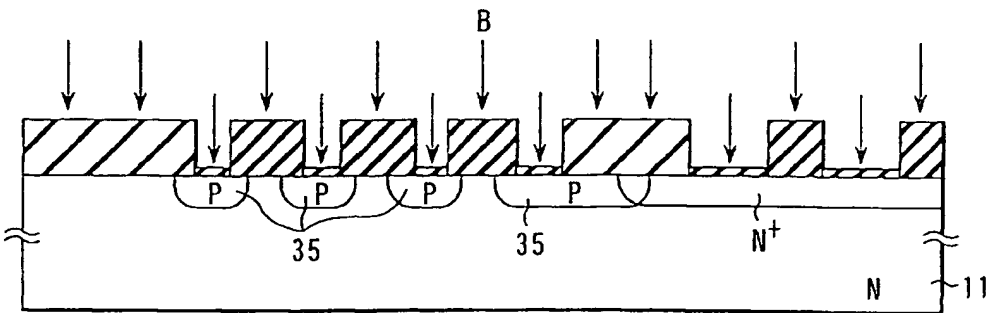


FIG. 14

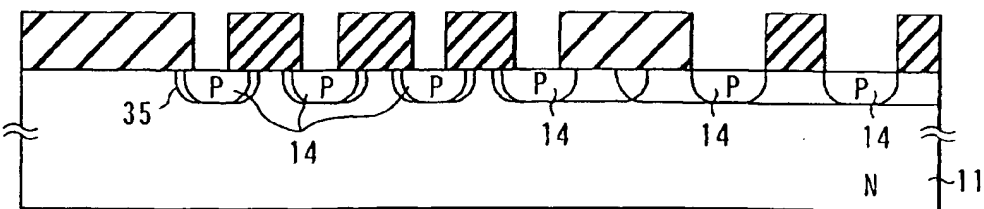


FIG. 15

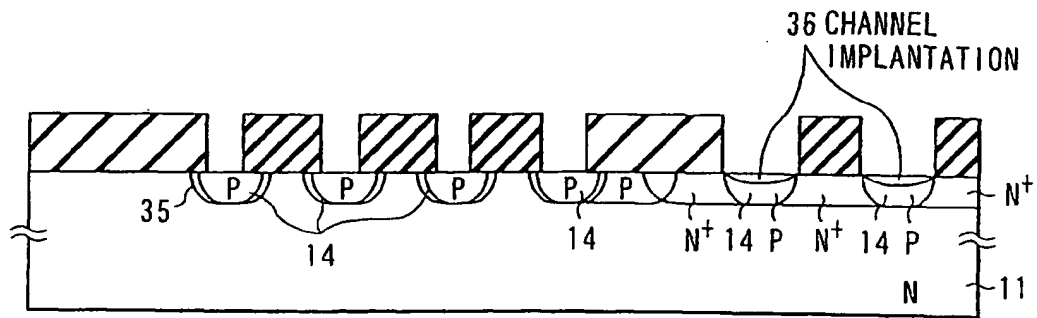


FIG. 16

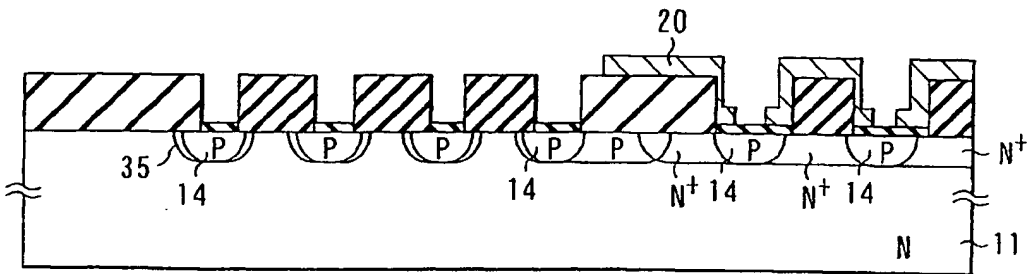


FIG. 17

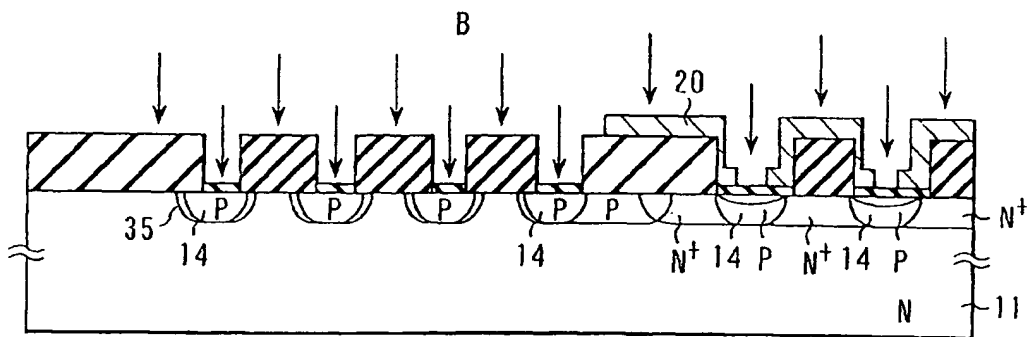


FIG. 18

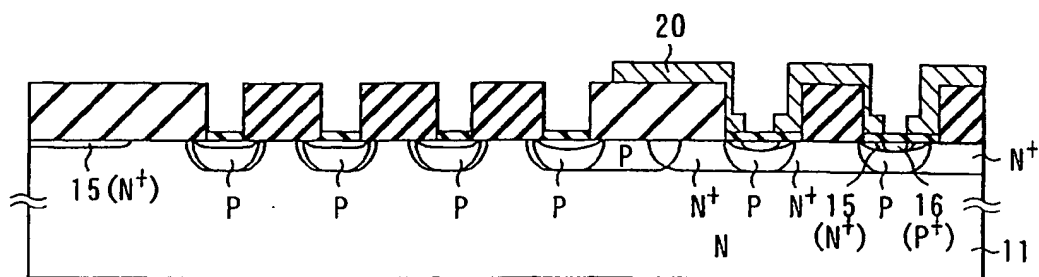


FIG. 19

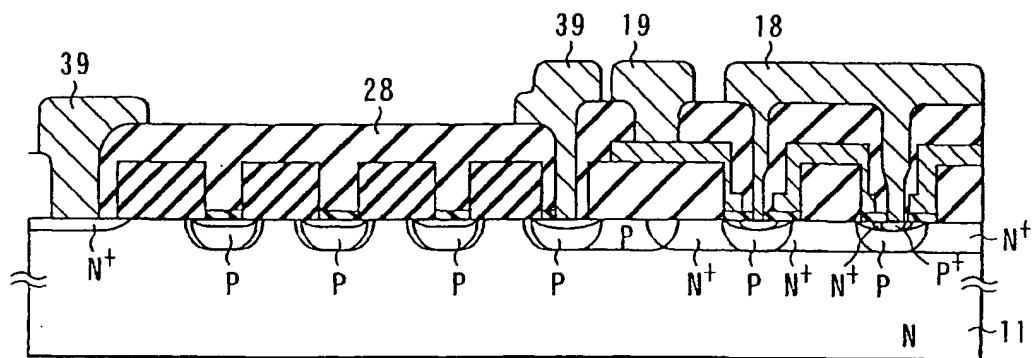


FIG. 20

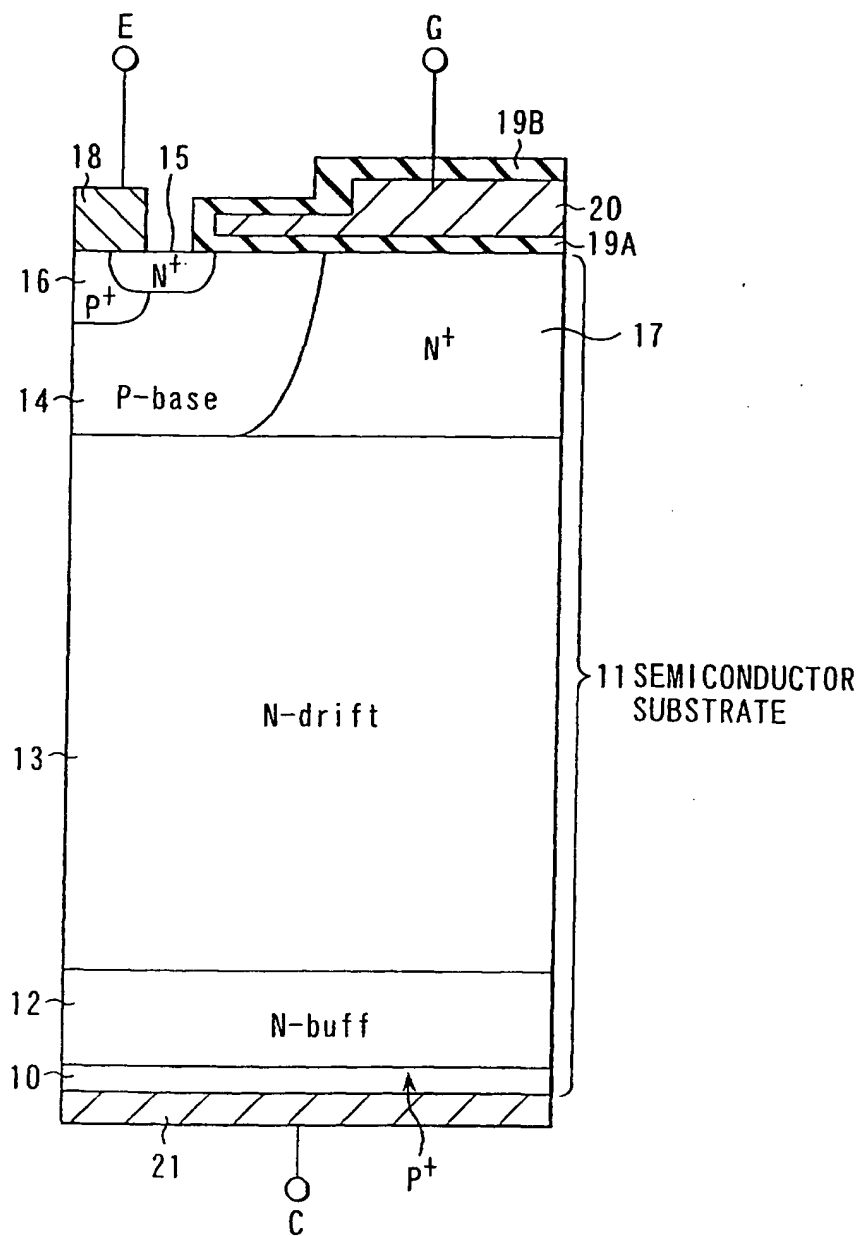


FIG. 21

FIG. 22

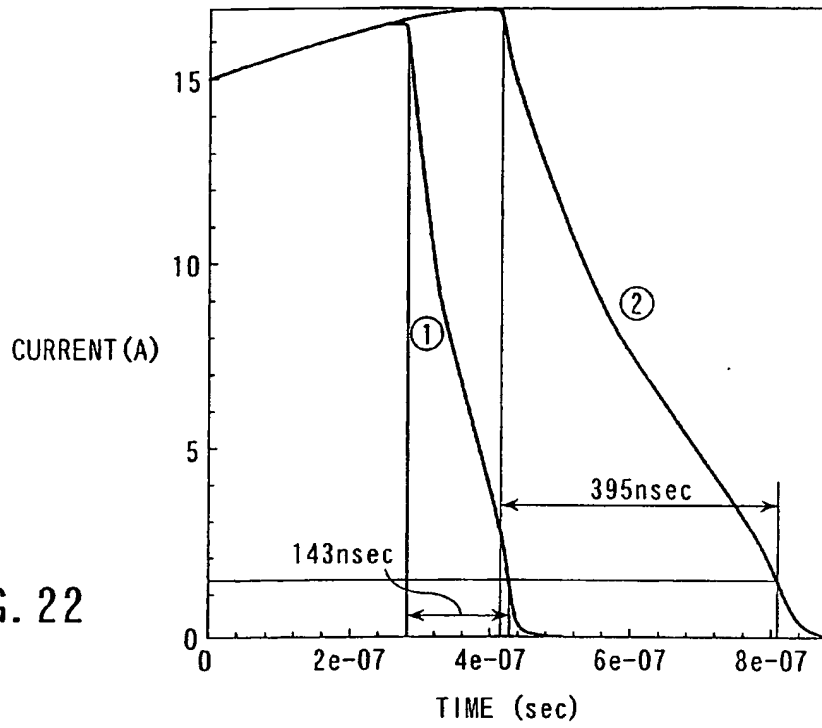


FIG. 23

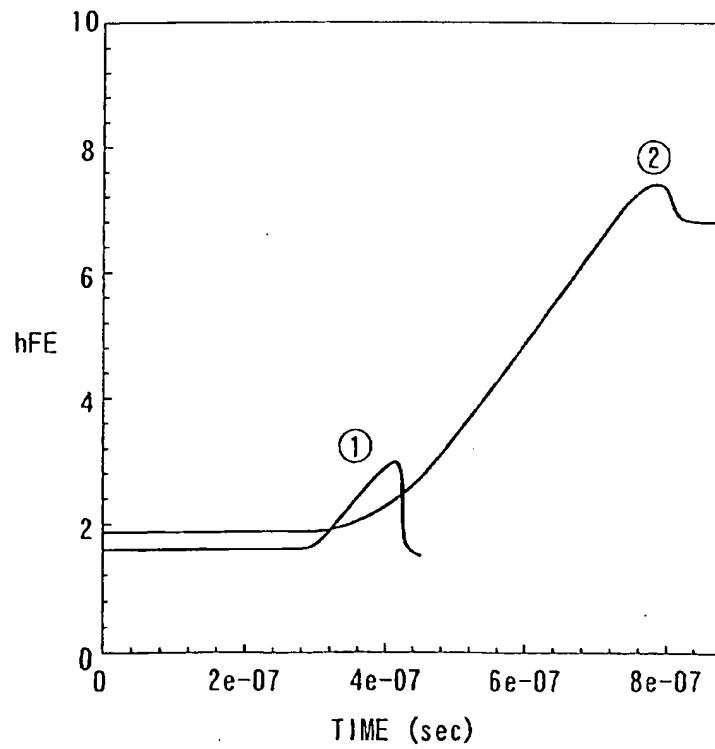


FIG. 24

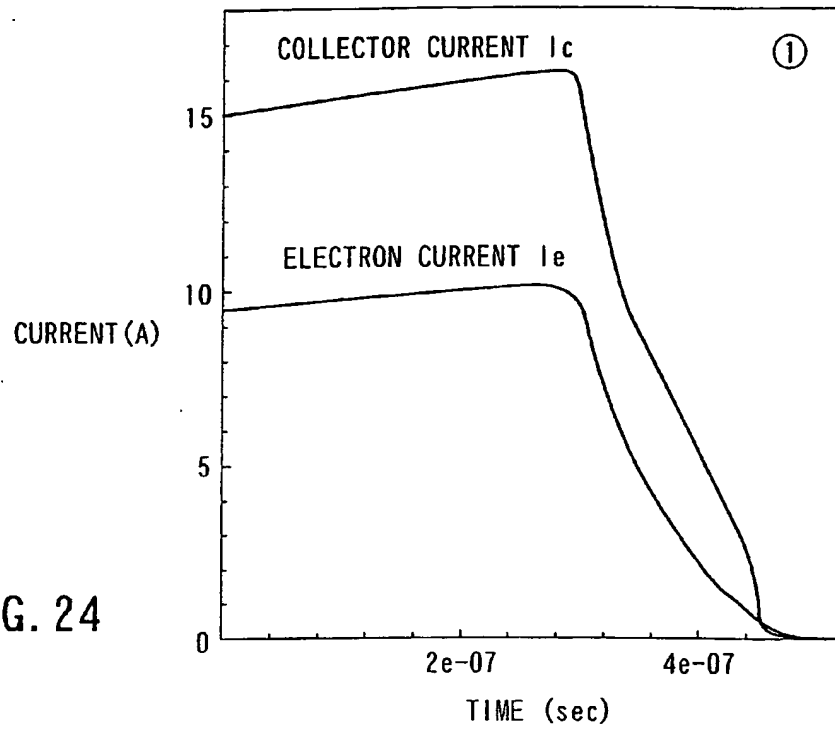
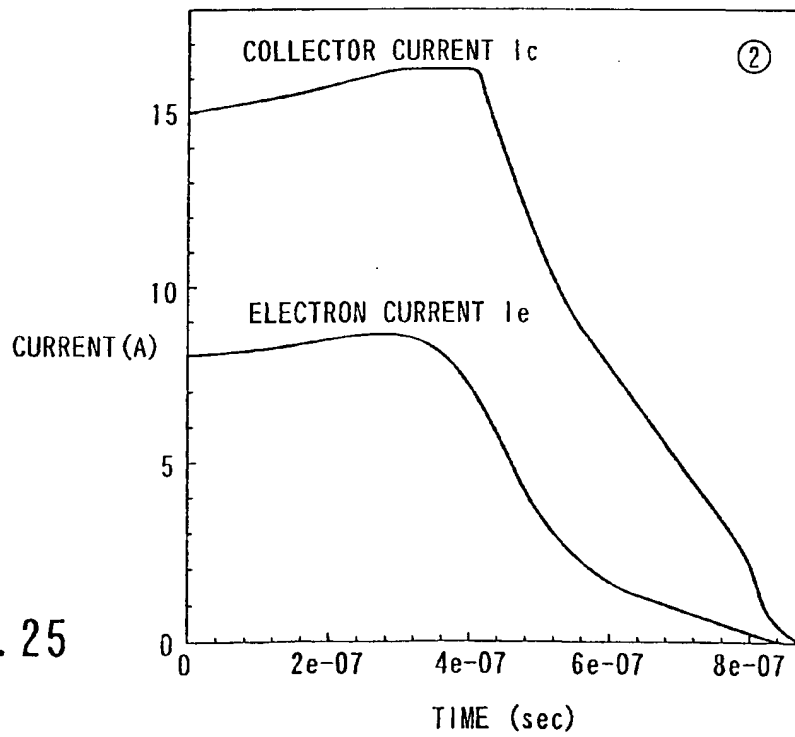


FIG. 25



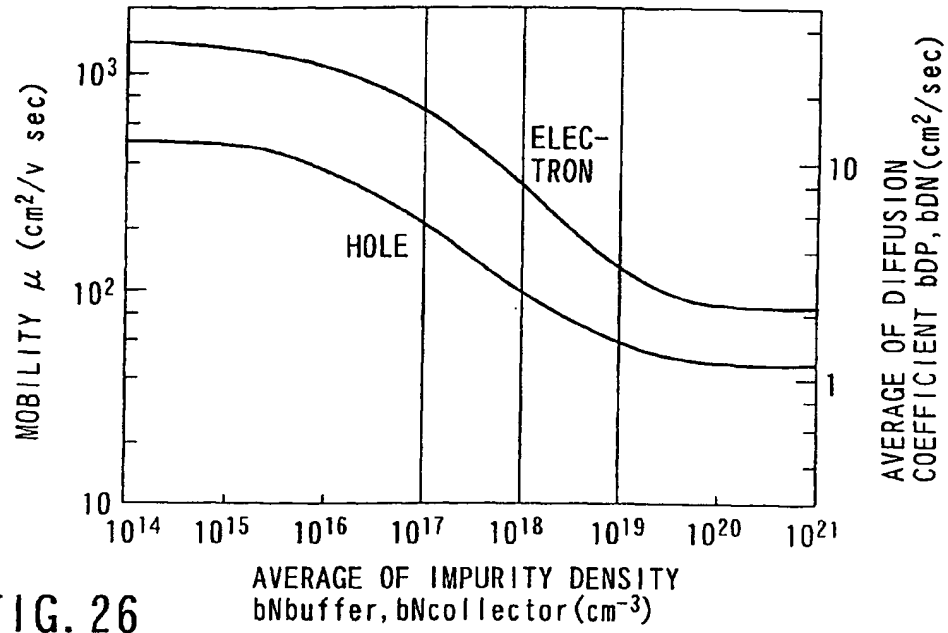


FIG. 26

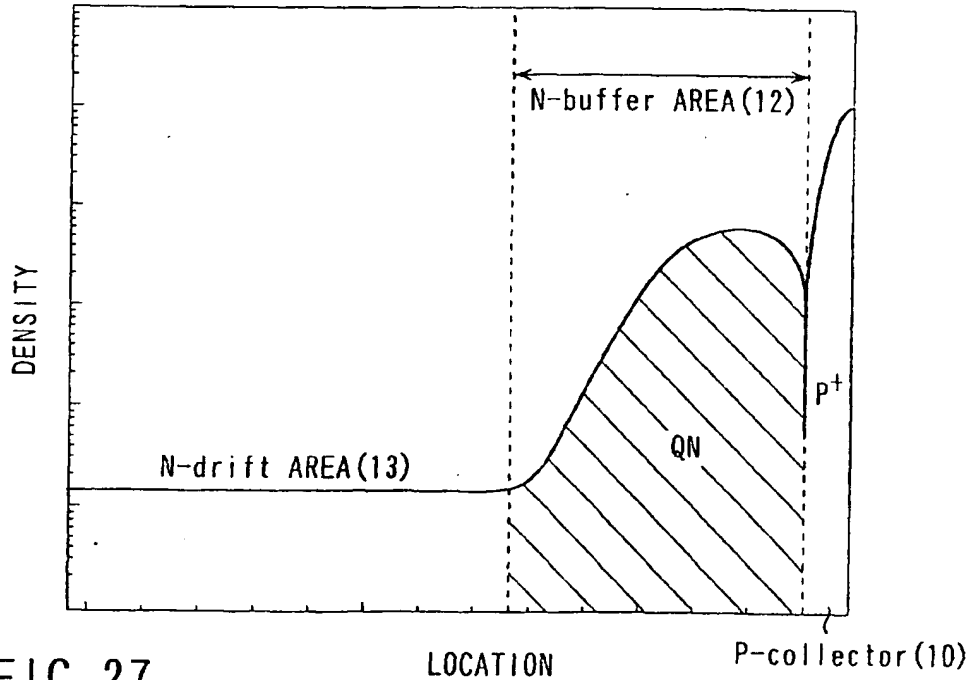


FIG. 27